ABSTRACT OF THE DISCLOSURE

A programmable driver/equalizer with an alterable FIR enables the equalization of serial links or other transmission systems to adapt to a variety of transmission media and impairments specifically, intersymbol interference (ISI). Current mode differential drive circuits are coupled to a transmission media via a Finite Impulse Response (FIR) filter operating in the Z transform mode. The filter transfer function is of the general form of $H(Z) = AB_0 + AB_1Z^{-1} + AB_2Z_2Z^{-2} + AB_nZ^{-n}$. The driver circuit is coupled to A and B coefficient setting circuits for the filter. The driver circuit also includes A coefficient level driver compensation and B coefficient level driver compensation to reduce the self-induced ISI from the driver while the filter coefficients are activated. The driver includes logic to further reduce ISI by switching off high capacitance paths when the filter coefficients are inactive. A driver bias circuit includes a current mirror, which feeds a reference current to the equalizer. The filter circuit comprises delay circuits responsive to the A and B coefficients. The delay circuits are additively connected together between the input and output of the filter. Each delay circuit includes a shift register containing the current outgoing data bit and a history of three previous bits. The shift registers in turn control the action of the weighted current drivers. The coefficient setting circuit receives a combination of control bits to select the appropriate response for the driver to the various transmission media parameters. Adjustments to the driver output current are made at data run lengths exceeding certain values and subsequent adjustments are made for data run lengths exceeding larger values. The adjustments are made to optimize the equalization for multiple environments and frequency transfer functions. When coefficients are used, a self-induced ISI from the driver is minimized by the driver strength of the output stage. When coefficients are inactive, ISI is minimized by switching off the paths to the high capacitance nodes in the circuit. The output peak amplitude is

constant by design of the driver circuits, enabling the power settings to be used for all possible coefficient possibilities.